PATENT W&B Ref. No.: INF 2227-PC/US Atty. Dkt. No. INFN/W80060

IN THE CLAIMS:

Please cancel claims 1-3 and 7-15 without prejudice and amend the claims as follows:

- 1-3. (Canceled)
- 4. (Currently Amended) The programmable read-only memory cell of claim-2, A programmable read-only memory cell, comprising:
 - a source electrode;
 - a drain electrode;
 - a channel layer formed between the source electrode and the drain electrode;
 - a floating gate isolated from the channel layer; and
- a selection gate isolated from the channel layer, wherein the selection gate and the floating gate are arranged on opposite sides of the channel layer, and wherein a first insulator layer is arranged between the floating gate and the channel layer and a second insulator layer is arranged between the selection gate and the channel layer;

wherein the floating gate is arranged at least partly in a trench of a substrate, wherein the trench is formed between the source electrode and the drain electrode, and wherein the floating gate is electrically insulated from the substrate; and

wherein a trench capacitor is formed in the substrate, an inner electrode of said trench capacitor being formed by the floating gate and an outer electrode of said capacitor being formed by a first diffusion region.

- 5. (Original) The programmable read-only memory cell of claim 4, wherein the first diffusion region is formed within a second diffusion region and the second diffusion region is formed within a third diffusion region, the second diffusion region having a complementary doping with respect to the first diffusion region and with respect to the third diffusion region.
- 6. (Original) The programmable read-only memory cell of claim 4, wherein the first diffusion region of the read-only memory cell has an overlap region with one or

Page 2

W&B Ref. No. : INF 2227-PC/US Atty. Dkt. No. INFN/WB0060

more first diffusion regions of two read-only memory cells of a matrix-type arrangement of read-only memory cells that are directly adjacent in a direction perpendicular to a word line, and wherein the overlap region forms an electrically conductive connection between the first diffusion regions of a plurality of read-only memory cells in a series.

PATTERSON&SHERIDAN

7-15. (Canceled)

- 16. (Currently Amended) The programmable read-only memory cell of claim 15, further-A programmable read-only memory cell, comprising:
 - a floating gate disposed in a trench of a substrate;
- a channel layer formed over the floating gate, connecting a source electrode to a drain electrode;
 - a selection gate disposed above the channel layer;
 - a first insulator layer disposed between the floating gate and the channel layer;
- a second insulator layer disposed between the selection gate and the channel layer:
 - an insulator layer disposed between the floating gate and the substrate; and
- a trench capacitor, formed in the substrate, comprising an inner electrode formed by the floating gate and an outer electrode formed by a first diffusion region disposed between the insulator layer and the substrate.
- 17. (Original) The programmable read-only memory cell of claim 16, further comprising:
 - a second diffusion region surrounding the first diffusion region; and
- a third diffusion region surrounding the second diffusion region, wherein the second diffusion region has a complementary doping with respect to the first diffusion region and with respect to the third diffusion region.
- 18. (Original) The programmable read-only memory cell of claim 17, wherein the first diffusion region has one or more overlap regions with one or more adjacent first diffusion regions of adjacent read-only memory cells in a direction perpendicular to a

PATENT W&B Ref. No. : INF 2227-PC/US Atty. Dkt. No. INFN/WB0060

word line, and wherein the one or more overlap regions form an electrically conductive connection between adjacent first diffusion regions.

PATTERSON&SHERIDAN

- 19. (Original) The programmable read-only memory cell of claim 17, wherein the channel layer is formed as an epitaxial layer having an n-type doping, and wherein the channel layer is isolated from the floating gate and the selection gate.
- The programmable read-only memory cell of claim 17, wherein the 20. (Original) source electrode and the drain electrode are formed at least partly on a surface of a substrate.